



Logic Gates Made from Polymer Transistors and Their Use in Ring Oscillators

A. R. Brown; A. Pomp; C. M. Hart; D. M. de Leeuw

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are seasonal features observed in both the trace species and isotopic altitudinal profiles. Further measurements may define both the source of the anomalous fractionations and the seasonal character.

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ysis, for O_2 the error is ± 0.04 per mil for $\delta^{18}\text{O}$ and 0.08 per mil for $\delta^{17}\text{O}$. The amount of O_2 measured from the different flights was identical; thus, the error is assumed to be the same.

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Logic Gates Made from Polymer Transistors and Their Use in Ring Oscillators

A. R. Brown,* A. Pomp, C. M. Hart, D. M. de Leeuw

Metal-insulator-semiconductor field-effect transistors have been fabricated from polymer semiconductors that can be processed from solution. The performance of these transistors is sufficient to allow the construction of simple logic gates that display voltage amplification. Successful coupling of these gates into ring oscillators demonstrates that these logic gates can switch subsequent gates and perform logic operations. The ability to perform logic operations is an essential requirement for the use of polymer-based transistors in low-cost low-end data storage applications.

One major application for polymeric metal-insulator-semiconductor field-effect transistors (MISFETs) (1–4) is in low-end data storage, such as chip cards and identification tags. Here the use of crystalline silicon technology is inappropriate: The excellent electrical performance of silicon, in terms of switching speed and small volume, is not required, and the bonding of silicon chips onto flexible plastic substrates dominates costs. The component parts of a MISFET are an insulator layer, conducting contacts, and a semiconductor layer. Soluble organic insulators are well known [such as poly(methyl methacrylate) and poly(vinyl chloride)], and recently Garnier *et al.* (2) have demonstrated that conducting contacts for such polymer MISFETs can be achieved by printing techniques. If a solution-processible organic semiconductor is also used, low-cost large-area electronics for data storage can be realized by using only printing processing steps directly onto plastic substrates (rendering ex-

pensive photolithographic steps obsolete and avoiding incompatibility problems).

However, electronic circuits with a polymer as the active semiconductor have not been reported. Until now, polymer MISFETs have not been able to display voltage amplification, which is a fundamental requirement for the construction of useful logic gates. Only if the logic gates can switch subsequent gates does integration become

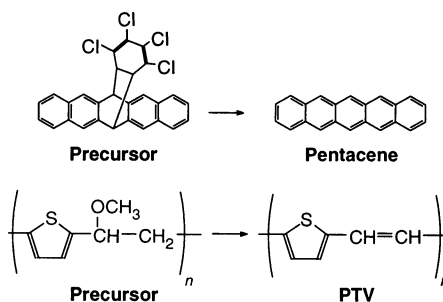


Fig. 1. Chemical structures of pentacene, PTV, and their precursors. Both elimination reactions occur at 140°C for 1 hour; pentacene is realized in vacuo and PTV in N_2 and HCl .

possible. We report here on the successful construction of polymer MISFETs that do display voltage amplification. Two different solution-processible organic semiconductors were used. The MISFETs have been used to fabricate both inverter and NOR gates. Switching of one gate by another is demonstrated in ring oscillators constructed from five identical coupled stages.

These gates have been realized with the use of precursor-route through-conjugated polymers. Through-conjugated polymers are intractable, being neither soluble nor fusible. Solution processibility has been successfully introduced to conjugated polymers such as polythiophenes and poly(paraphenylenes) by the introduction of solubilizing side chains (for example, alkyl and alkoxy groups). However, these side chains have a detrimental effect on the charge-carrier mobility because they both decrease through-conjugation (1) and decrease π - π overlap of neighboring chains (5). In a precursor route, solubilizing side chains are chosen that can be eliminated later to leave only the through-conjugated polymer. Hence, precursor polymers are particularly suited to be the active semiconductor in polymeric MISFETs, combining solution processibility with good electrical properties (6). Here we use oligomeric pentacene and fully polymeric poly(thienylenevinylene) (PTV),

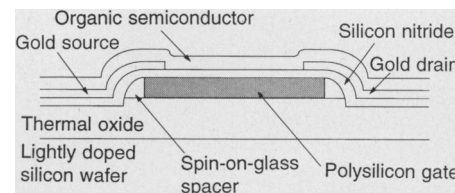


Fig. 2. Schematic cross section of transistors used in this study.

Philips Research Laboratories, Professor Holstlaan 4, 5656 AA Eindhoven, Netherlands.

*To whom correspondence should be addressed.

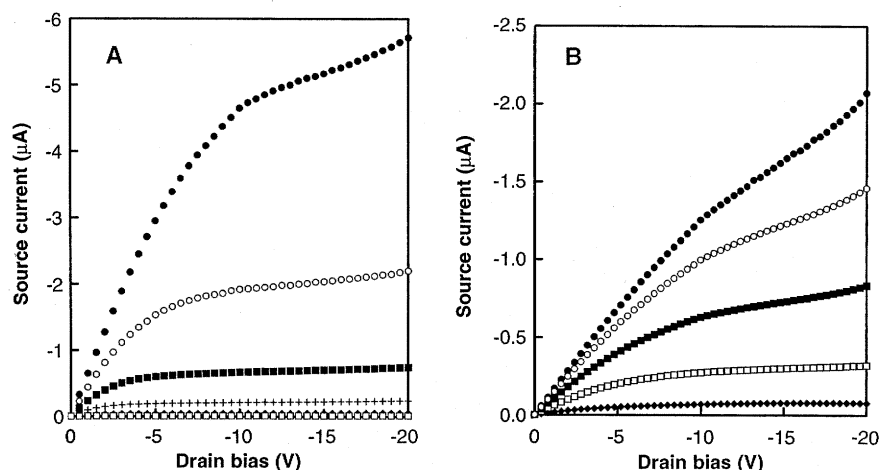


Fig. 3. Typical transistor characteristics of (A) a pentacene MISFET and (B) a PTV MISFET. Drain biases were swept from -20 to 0 V. The pentacene MISFET was measured at gate biases of -20 V (●), -18 V (○), -16 V (■), -14 V (+), -12 V (◆), and -10 V (□). The PTV MISFET was measured at gate biases of -20 V (●), -15 V (○), -10 V (■), -5 V (□), and 0 V (◆). For both MISFETs, $W = 10$ mm and $L = 16$ μm . Gate to source-drain overlap was 2 μm .

which are both processed by soluble-precursor routes (7, 8) (Fig. 1). Thin films (~ 100 nm) of both precursors are readily produced by spin-coating from common organic solvents such as dichloromethane.

Because the aim of this study was to evaluate the performance of the organic semiconductors, transistor substrates were, for simplicity, constructed by conventional photolithographic techniques. On top of a lightly n -doped silicon wafer with a thermal oxide coating (0.5 μm), heavily phosphorus-doped polysilicon gate contacts (0.35 μm) were deposited and patterned (Fig. 2). After planarization with spin-on-glass spacers, silicon nitride gate insulator (100 nm) was deposited by low-pressure chemical vapor deposition. Gold (200 nm) was vacuum deposited and patterned for source and drain contacts. Channel lengths L ranged from 8 to 26 μm , channel widths W were either 10 or 30 mm, and the gate to source-drain mask overlap was 2 or 20 μm . The mask design included individual transistors

and integrated transistor-transistor connections for logic gates. Logic gates were arranged 1 mm apart, and consequently, leakage currents between gates through the unpatterned polymer film were negligible, being at least 2 orders of magnitude smaller than device currents.

Transistor characteristics for typical pentacene and PTV transistors are shown in Fig. 3. Both semiconductors are p -type, with current enhancement at negative gate biases. The mobility μ of charge carriers in the MISFETs was measured in the linear regime (9). On substrates with silicon dioxide as the insulator, we have optimized the field-effect mobility of pentacene in MISFETs to a value of 10^{-2} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. On the present substrates, however, the maximum observed mobility is 10^{-3} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. For the PTV MISFETs, the mobility is equal to 10^{-4} $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. The conductivities of the films are 10^{-5} and 2×10^{-6} S cm^{-1} for pentacene and PTV, respectively. The ratio of the field-effect mobility to the conductivity exceeds that found

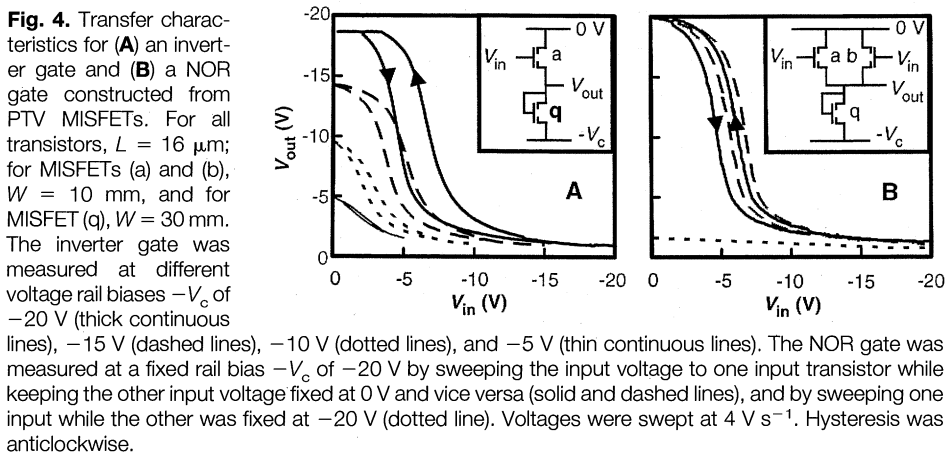


Fig. 4. Transfer characteristics for (A) an inverter gate and (B) a NOR gate constructed from PTV MISFETs. For all transistors, $L = 16$ μm ; for MISFETs (a) and (b), $W = 10$ mm, and for MISFET (q), $W = 30$ mm. The inverter gate was measured at different voltage rail biases $-V_c$ of -20 V (thick continuous lines), -15 V (dashed lines), -10 V (dotted lines), and -5 V (thin continuous lines). The NOR gate was measured at a fixed rail bias $-V_c$ of -20 V by sweeping the input voltage to one input transistor while keeping the other input voltage fixed at 0 V and vice versa (solid and dashed lines), and by sweeping one input while the other was fixed at -20 V (dotted line). Voltages were swept at 4 V s^{-1} . Hysteresis was anticlockwise.

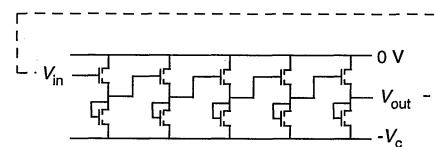


Fig. 5. Schematic of an inverter ring oscillator constructed from five inverter gates.

in ordinary soluble conjugated polymers (10) and gives rise, at low gate biases, to clear current saturation at drain biases above -10 V. Hence, the channel transconductance

$$\frac{\partial I_{sd}}{\partial V_g} \Big|_{V_d = \text{const}}$$

exceeds the channel conductance

$$\frac{\partial I_{sd}}{\partial V_d} \Big|_{V_g = \text{const}}$$

(s , d , and g are the source, drain, and gate), which is the prerequisite for voltage amplification in electronic circuits. Devices with gate to source-drain overlap of only 2 μm had characteristics identical to those with an overlap of 20 μm ; because of their reduced stray capacitance, the devices with smaller overlap were preferred for logic-gate construction.

The simplest gate, a voltage inverter, constructed with PTV transistors displayed clear inverter logic operation (Fig. 4A). Similar results were obtained with pentacene transistors. Different values for the negative circuit voltage rail $-V_c$ were used. An input voltage V_{in} of $-V_c$ yielded an output voltage V_{out} of 0 V; an input voltage of 0 V yielded an output voltage of $-V_c$. More importantly, for negative voltage rails of -10 V and above in magnitude, voltage amplification ($|dV_{out}/dV_{in}| > 1$) was observed at the switching point of the input-output characteristics, in agreement with the transistor characteristics. The anticlockwise hysteresis was probably the result of charge trapping in the silicon nitride (11).

Correct NOR logic operation was observed for a NOR gate constructed from three PTV MISFETs (Fig. 4B). An output voltage of 0 V was observed when either input or both inputs equaled -20 V; an output voltage of -20 V was observed only when both inputs equaled 0 V. The similarity of the input-output characteristics when one input voltage was held at 0 V and the other was swept indicates that transistors are reproducible. Voltage amplification was again observed.

Logic gates displaying voltage amplification can be used to drive subsequent gates without losing logic integrity: the output voltage will always be close to either 0 V or $-V_c$. Coupled logic gates without voltage amplification tend to yield the ambiguous logic-state output $-V_c/2$. To demonstrate the ability of the polymer logic gates to drive subsequent gates, we constructed ring

oscillator circuits. For an inverter oscillator (Fig. 5), we coupled five inverters together, with the output voltage of one inverter providing the input for the following. If the initial input to the first inverter is 0 V ($-V_c$), then the output of the fifth will be $-V_c$ (0 V). Returning the output of the fifth inverter as the input for the first inverter causes all of the inverters to sequentially change logic state. Consequently, the circuit oscillates with a characteristic frequency f_{osc} . If all transistors are identical, f_{osc} is $1/10$ of the switching delay frequency of an individual inverter. In reality, f_{osc} is limited by the slowest gate. For pentacene ring oscillators, f_{osc} is in the range of 100 to 500 Hz, and for PTV ring oscillators, f_{osc} is in the range of 10 to 50 Hz. These values are dominated by the RC time constant of the channel resistance R of the load transistor (the nonswitching transistor), which is given by $R \approx L/\mu WC_{ins}V_d$, and the channel capacitance C , which is given by $C = LWC_{ins}$, where C_{ins} is the capacitance per unit area of the insulator. During the oscillations, the drain bias V_d of the load transistor constantly varies between 0 V and $-V_c$, and thus, the channel resistance also varies. The measured frequencies are thus as expected, being lower but within an order of magnitude of the maximum transit frequency for a carrier between the source and drain contacts of a MISFET, $f_{transit} \approx \mu V_d/L^2$. Because mobilities as high as $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ have been reported (1, 2), switching frequencies as high as 50 kHz are to be expected. More complicated NOR gate oscillators have also been successfully constructed. Here, in each of the NOR gates, one of the two inputs is held at 0 V, while the other input is provided by the output of the previous gate.

The observation of ring oscillations indicates that there is good reproducibility of the transistors, because each ring oscillator requires that all 10 transistors operate within given specifications. Devices are measured in air without encapsulation. A pentacene oscillator operating at 130 Hz has been observed to oscillate continuously for 24 hours, which represents in excess of 10^7 switching operations. Shelf lifetimes of both pentacene and PTV devices are at least an order of magnitude longer.

Through-conjugated polymers are thus suitable as the active semiconductor in cheap integrated electronic circuits. In order to replace the silicon-based substrates of this study and successfully produce electronic circuits by printing techniques, attention must now be directed toward the reliable printing of micrometer-scale conducting tracks.

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Optical Microfabrication of Chalcogenide Glasses

H. Hisakuni and K. Tanaka*

It was found that chalcogenide glasses can be shaped by stressing the glass under light illumination because light illumination enhances the fluidity of the glass. The mechanism of photoinduced fluidity was found to be photoelectronic, that is, athermal. The process can be applied to microfabrication of optical fibers and glassy films with a typical dimension of 10 to 100 micrometers.

Unlike crystalline materials, glass can be shaped into arbitrary forms at supercooled states. In the supercooled state, glass has a viscosity of less than $\sim 10^{13}$ poise (1–3) and has moderate fluidity. Such a fluid state can be attained by heating a glass above the glass transition temperature (1–3). Here, we demonstrate that the fluid state can be obtained by an athermal process, through illumination with visible light. We have observed photoinduced fluidity in several kinds of chalcogenide glasses and describe here the characteristics of a representative chalcogenide glass As_2S_3 (2, 4) in a photoinduced fluid state.

Optically processed As_2S_3 glass is shown in Fig. 1. In Fig. 1A, the sample is 50 μm in thickness and approximately 0.2 mm by 2 mm in lateral dimension. The sample was prepared through vacuum evaporation and then annealed at the glass transition temperature (~ 450 K), a process commonly used for stabilizing glass structures (2). Next, one end of the sample was pasted to a glass slide, and the other end was bent with a stick. We confirmed that the bending was elastic because the deformed glass recovered when the stress was removed. However, when the bent glass flake was illuminated locally by focused light, permanent deformation occurred (Fig. 1A). The illuminated part, indicated by an arrow in the figure, becomes viscous, and the sample is bent segmentally. In Fig. 1B, an As_2S_3 optical fiber with a diameter of 100 μm was illuminated with focused light and subject-

ed to elongated stress. Only the illuminated position becomes viscous, and as a result, it becomes constricted. In these two examples, we see that the deformations are restricted to a scale of $\sim 100 \mu\text{m}$, which corresponds to the focused light spot. Such local deformations of glasses may be very difficult to achieve with thermal techniques (2, 5) because of heat conduction.

To understand the mechanism of photoinduced fluidity, we measured the fluidity (the inverse of the viscosity) in As_2S_3 glass under illumination. The fluidity was evaluated through a creep measurement (2, 6). A typical result is shown in Fig. 2. In the dark no appreciable elongation occurred, but under illumination from a He-Ne laser, the length of the flake increased dramatically.

The viscosity η can be defined as

$$de/dt = \tau/\eta \quad (1)$$

where e is the viscous strain and τ is the stress (2, 6). Using this equation, we calculate that $\eta \geq 10^{14}$ poise in the dark and $\eta \approx 5 \times 10^{12}$ poise under illumination. This viscosity value is consistent with the deformation shown in Fig. 1. We also confirmed that the viscosity decreases with increasing light intensity.

The temperature dependence of the viscosity of As_2S_3 is shown in Fig. 3. In the dark at approximately room temperature, the viscosity of As_2S_3 flakes cannot be measured, which means that $\eta \geq 10^{14}$ poise. In contrast, the viscosity of the illuminated sample increases at higher temperatures, that is, the photoinduced fluidity becomes less appreciable at higher temperatures.

The temperature dependence shown in Fig. 3 strongly suggests that the photoin-

Department of Applied Physics, Faculty of Engineering, Hokkaido University, Sapporo 060, Japan.

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