Self-Aligned, Vertical-Channel, Polymer Field-Effect Transistors

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Self-Aligned, Vertical-Channel, Polymer Field-Effect Transistors

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The manufacture of high-performance, conjugated polymer transistor circuits on flexible plastic substrates requires patterning techniques that are capable of defining critical features with submicrometer resolution. We used solid-state embossing to produce polymer field-effect transistors with submicrometer critical features in planar and vertical configurations. Embossing is used for the controlled microcutting of vertical sidewalls into polymer multilayer structures without smearing. Vertical-channel polymer field-effect transistors on flexible poly(ethylene terephthalate) substrates were fabricated, in which the critical channel length of 0.7 to 0.9 micrometers was defined by the thickness of a spin-coated insulator layer. Gate electrodes were self-aligned to minimize overlap capacitance by inkjet printing that used the embossed grooves to define a surface-energy pattern.

Many advanced electronic device configurations, such as vertical transistors (*1*) and vertical-cavity surface-emitting lasers, require the formation of well-defined vertical sidewalls in functional multilayer structures. Most conventional techniques for fabrication of such sidewalls are based on photolithographic patterning followed by either reactive ion etching or anisotropic wet chemical etching. Application of these techniques to polymer multilayer structures is difficult because of plasma-induced degradation of electroactive polymers and the lack of anisotropic etching techniques for polymers.

Different patterning techniques for low-cost fabrication of solution-processible polymer field-effect transistors (FETs) have been demonstrated, including photolithographic patterning (*2*), screen printing (*3*), soft lithographic stamping (*4*), micromolding in capillaries (*5*), and high-resolution inkjet printing (*6*). These techniques allow accurate definition of polymer patterns with micrometer resolution, but they do not permit the formation of vertical sidewalls and, with some exceptions such as near-field photolithography (*7*), their extension to submicron resolution patterning is complex and becomes more expensive the higher the required resolutions.

Embossing is a nonlithographic patterning technique that has found widespread industrial use in the manufacture of diffraction gratings, compact disks, and security features such as holograms (*8*), but that is also capable of imprinting nanoscale patterns into single, sacrificial polymer layers that can be transferred subsequently into a functional layer by conventional etching (*9*). The LIGA technique (a German abbreviation for lithographic galvanic deposition) that is widely used for fabrication of micro-electrical-mechanical structures is based on the embossing of high-aspect-ratio structures in poly(methyl methacrylate) (PMMA) (*10*). Direct laser-assisted imprinting of silicon surface layers has been demonstrated (*11*). Plastic substrates containing conventional organic transistors have been molded in order to reduce the surface area taken up by the transistors (*12*). Here we show that the recently developed technique of microcutting by solid-state embossing (*13*) can be used to accurately microcut through multilayer structures that contain several electroactive layers such as conducting electrodes. This enables the fabrication of new device configurations based on controlled formation of vertical sidewalls in polymer multilayers. We demonstrate the fabrication of planar-channel and vertical-channel polymer FETs on cheap, flexible poly(ethylene terephthalate) (PET) substrates. The key feature of a vertical-channel polymer FET is that the channel length is defined by simple control of the thickness of a film (*1*), and not by a high-resolution submicrometer lithography step. This approach provides a low-cost manufacturing technique for submicrometer FETs, based on solution processing and direct printing.

The process consists of forcing a microcutting tool that comprises an array of sharp protruding wedges into a multilayer structure of one or more electrically conductive layers on a PET substrate. For the planar-channel FETs (Fig. 1A, left column), a single conducting layer for the source-drain electrodes is deposited on top of the substrate. Electrodes are coarse-patterned by inkjet printing of the conducting polymer, poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonic acid) (PEDOT/PSS), or alternatively by shadow-mask evaporation of gold. During the microcutting, the substrate is held just below its glass transition temperature, T_g (for PET with $T_g \approx 80°C$, $T_{emboss} \approx 70$ to $75°C$, where T_{emboss} is the temperature of the substrate when embossing occurs), and a nominal pressure of $\sim$100 g mm^{-2} is applied for 30 to 60 min, so that a V-shaped microgroove cutting the metal layer is formed (Fig. 1A, left column) (*14*). The embossing time can be shortened with higher load pressure. Subsequently, layers of polymer semiconductor and gate insulator are deposited conformally into the microgroove by spin-coating. Swelling of underlying layers can be avoided with the proper choice of solvents and processing parameters. Semiconducting poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) (*15*) or regioregular poly(3-hexylthiophene) (P3HT) (*16*) was deposited from a 0.3 weight percent (wt %) (F8T2) and 0.7 wt % (P3HT) solution in m-xylene (*17*). The gate dielectric poly(vinylphenol) (PVP) was deposited from a 10 wt % solution in isopropanol, and finally, a top-gate electrode was applied. The master comprised sharp protruding wedges of height $h \sim 10$ μm, angle $\alpha = 70°$, and periodic distance between wedges, Λ, of 500 μm, producing 5- to 10-μm deep cuts (Fig. 1B) and planar channel length $L \approx 12$ to 17 μm.

Because downscaling of L improves switching speed, we also set out to fabricate vertical-channel FETs, in which the channel length would be defined by the thickness of a deposited insulating polymer layer rather than by the master geometry. First, we fabricated a trilayer structure consisting of two coarse-patterned electrode layers, separated by a thin polymer insulator layer, by depositing thin gold or PEDOT pads onto a PET substrate, spin-coating a 0.5- to 1-μm PVP layer from isopropanol, and applying another

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slightly shifted set of gold or PEDOT electrodes (Fig. 1A, right column). Subsequently, the conductor/insulator/conductor triple-layer supported by the PET substrate was microcut with the same process parameters as above. In this way, source-drain electrodes for two submicron, vertical-channel FETs (E1-E2 and E3-E4) and two planar source-drain pairs (E1-E3 and E2-E4) were fabricated simultaneously. In Fig. 1C, the thickness d of the PVP layer was measured to be 700 nm, leading to a channel length of $L \approx 900$ nm. The vertical devices were completed as described for the planar devices above, with PMMA spin-coated from a 10 wt % solution in butyl acetate as the gate dielectric.

Output and transfer characteristics of a representative vertical F8T2 FET fabricated with gold source (E1), drain (E2), and gate electrodes (Fig. 2, A and B) show a clean field effect with operation in *p*-type accumulation mode. The on-off current ratio of 10^3 is reasonably high, even in the saturation regime ($V_{ds} = -40$ V, where V_{ds} is the drain-source voltage), where a high electric field is present in the pinch-off region near the drain electrode of this short-channel device. In contrast to conventional planar F8T2 devices (*6*), the embossed vertical F8T2 FETs exhibit a superlinear dependence of the FET current on V_{ds} without current saturation. This is also present, although to a lesser degree, in the planar embossed devices (Fig. 2C). This is caused by nonohmic voltage drops across the embossed, charge-injecting F8T2/gold source-drain contacts, and is corroborated by the observation of a higher on-off current ratio when the top electrode E1 was the injecting source contact than when the bottom electrode E2 was the source.

In our experiments, we focused on a narrow range of PVP thicknesses (0.5 to 1 μm) in which deposition and embossing conditions were carefully optimized. To quantify the contact resistance, we analyzed the channel-length scaling by comparing the normalized current of embossed vertical-channel devices (L = 0.7 to 1.2 μm) (Fig. 2C, gray lines) with that of embossed planar-channel devices (black lines) and of reference FETs in a conventional planar configuration (*18*) (L = 2 to 20 μm). ($I_{ds}^* = I_{ds} \times L \times W^{-1}$, where I_{ds}^* is the normalized current and W is the channel width.) At high source-drain voltages, we observed clear scaling of the FET current with channel length. The field-effect mobilities extracted from the saturated transfer characteristics of planar and vertical embossed devices, as well as from reference F8T2 devices, are on the order of 2 to 3 × 10^{-3} cm^2 V^{-1} s^{-1} (*6*, *15*). However, at small V_{ds}, the normalized current in short-channel vertical devices is substantially smaller than that of long-channel planar devices. From channel-length scaling analysis (*19*), we extracted the current-voltage characteristics $I_c(V_c)$ of the parasitic source-drain contacts in series with the FET channel resistance. I_c follows an exponential dependence, $I_c = I_c^0 \times e^{\alpha V_c}$, on the voltage V_c, dropping across the contacts with a preexponential factor I_c^0 and $\alpha \simeq 0.25$ to 0.30 per volt (Fig. 2D). Similar behavior has been reported for the current-voltage characteristics in injection-limited hole-only polymer diodes (*20*). We conclude that at low V_{ds}, embossed F8T2 devices are injection-limited. I_c^0 depends on gate voltage, indicating that the contact resistance is reduced by the applied gate voltage (*21*). The source-drain contact resistance might be associated with the small contact area between F8T2 and buried electrodes E2 and E4 or with nonconformal coating of the semiconducting and dielectric polymers into the well. At the bottom of the groove, the layers will most likely be thicker than at the top because of surface-tension and capillary-force effects during spin-coating. Atomic force microscopy investigations of the topography of the grooves at various stages during the process have shown, however, that none of the deposited layers measurably planarizes the groove.

In order to minimize parasitic contact resistance, devices were also fabricated with P3HT as the active material. The ionization potential of P3HT ($I_p \approx 4.9$ eV compared to $I_p \approx 5.5$ eV for F8T2) is well matched to the work function of gold/PEDOT. For planar embossed P3HT devices, current saturation is clearly observable (Fig. 3A). The nonlinearities in the short-channel, vertical FET characteristics (Fig. 3B) can mostly be attributed to channel-length shortening effects (*1*) and to a lateral field dependence of the field-effect mobility (*19*). The $I_c(V_c)$ characteristics for embossed P3HT devices show that the contact resistance is negligible (Fig. 2D, squares) and comparable to that of conventional planar P3HT devices (*21*). Therefore, contact resistance problems are not inherent to the embossing process but can be overcome by a suitable choice of polymer semiconductor. The mobilities extracted from the saturated transfer characteristics of both planar and vertical microcut devices, as well as from reference P3HT devices, are approximately 0.01 cm^2 V^{-1} s^{-1}. Embossed P3HT devices exhibit stable and reproducible device characteristics. No hysteresis is observed between subsequent sweeps of the source-drain and gate voltage (V_g) (Fig. 3). The relatively high off currents at $V_g = 0$ V, observed for both the planar and the vertical device, are attributed to unintentional doping of the P3HT. This is typical also for conventional P3HT FETs in a top-gate configuration.

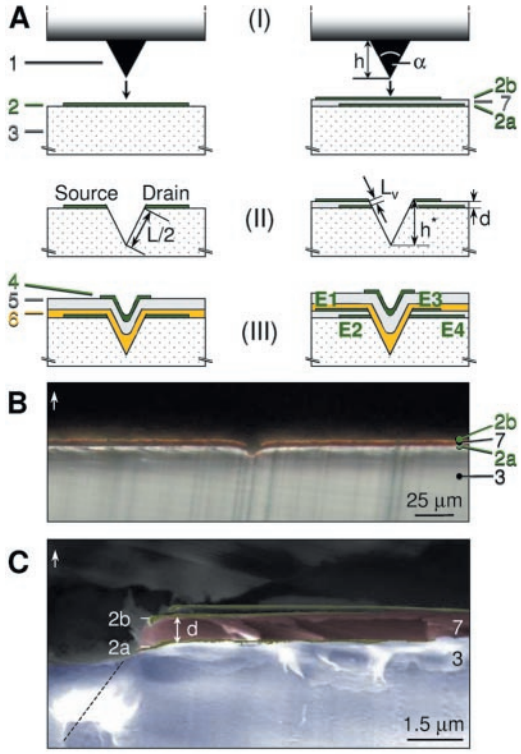

Fig. 1. (**A**) Fabrication steps for the manufacture of polymer FETs by microcutting. Left column, planar-channel FETs; right column, vertical FETs. In step 1, electrically conducting layer(s) (2), and for vertical FET fabrication an additional insulating separation layer (7), are structured on polymer substrates (3) by solid-state embossing (*22*) with a master with sharp protruding edges (1). In step 2, the top layer(s) (2a, 2b, and 7) are microcut, leading to accurately defined microelectrodes. In step 3, the devices are completed by application of a semiconducting layer (6), a gate insulator (5), and gate electrodes (4). (**B** and **C**) Optical and environmental scanning electron micrographs of a cross-section of a microcut triple layer on a PET substrate (3) with gold electrodes (2a and 2b) and a PVP dielectric (7). The top electrode layer (2b) is cut without smearing along the cutting direction. The bottom electrodes (2a) are not well recognizable. The indentation depth h^* is not deducible from the electron micrograph shown in (C). The cross-section was produced by microtoming, which possibly resulted in smearing of the PET substrate along the microtoming direction [indicated with the arrow at the upper left in (B) and (C)]. However, atomic force microscopy shows that h^* is much larger than the thickness of the triple layer (Fig. 4C). The expected shape of the groove is indicated by the dashed line in (C).

Structural characterization of the layers in the embossed grooves is challenging because of the difficulty in preparation of electron microscopy cross-sections of polymer multilayers. However, we have succeeded in obtaining optical and environmental scanning electron micrographs (Fig. 1, B and C) that clearly show that the microcutting process produces well-defined vertical sidewalls. No "smearing" of the top electrode along the indentation direction was observed. Unambiguous evidence for the integrity of the multilayer structure in the embossed grooves was obtained from electrical characterization: (i) The field-effect mobilities of planar and vertical-channel embossed devices with both F8T2 and P3HT were identical to those of reference devices fabricated in the same experiment with conventional planar lithographically defined devices. The field-effect mobility is a very sensitive measure of the electronic structure and interface roughness at the semiconductor-dielectric interface. (ii) No electrical shorts between top and bottom electrodes were generated. After microcutting, typical leakage currents between electrodes E1 and E2 were on the order of 1 nA or less (at a PVP thickness of 0.7 to 1.2 μm and an applied voltage of 40 V), which is comparable to leakage currents between electrodes E1 and E2 before the microcutting process. (iii) The transistor current of embossed vertical-channel P3HT devices with $L = 0.9$ μm was higher by about one order of magnitude than that of P3HT reference devices fabricated in the same experiment with a conventional device configuration with $L = 10$ μm (*18*), which was as expected from the reduction of channel length. The embossing method provides controlled, accurate definition of submicron critical-feature size without degradation of polymer field-effect mobility and results in substantial enhancement of FET drive-current capability.

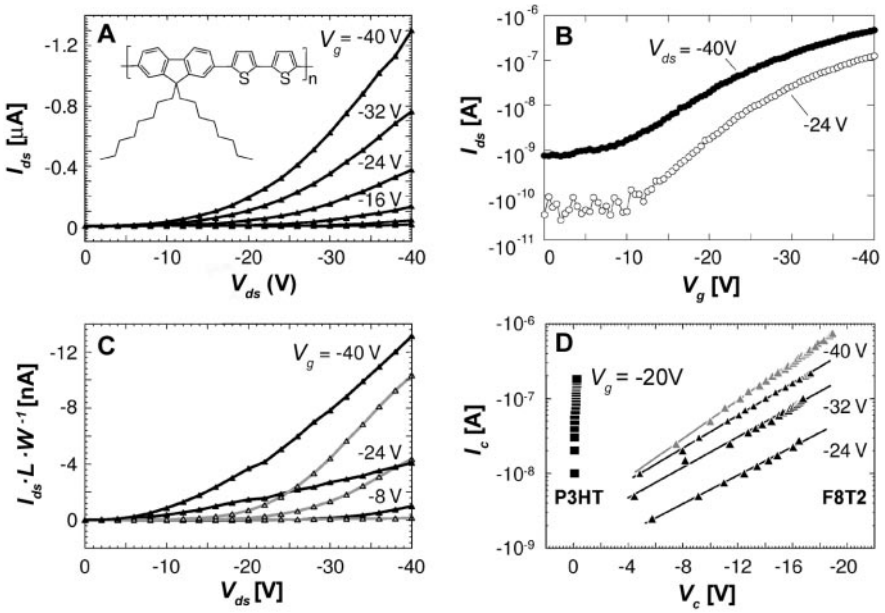

Fig. 2. Device performance of embossed F8T2 transistors. (**A** and **B**) Output characteristics (A) as a function of gate voltage (measured in steps of 8 V) and transfer characteristics (B) of a vertical device with gold source (E1), drain (E2), and gate electrodes ($L \approx 900$ nm; $W \approx 0.5$ mm). The inset in (A) shows the chemical structure of F8T2. (**C**) Normalized output characteristics of a vertical submicron-channel transistor with $L = 0.9$ μm (source-drain E1-E2, gray lines) and corresponding planar devices on the same set of electrodes ($L = 17.5$ μm) (source-drain E1-E3, black lines). (**D**) I_c-V_c characteristics of the source-drain contacts at different gate biases for two separate sets of microcut gold/F8T2 transistors (black and gray triangles) extracted from the scaling characteristics in (C). Gold/P3HT devices (squares) exhibit a substantially smaller contact resistance.

Another important factor in increasing transistor switching speed is the geometric overlap capacitance between the gate electrode and the source-drain electrodes. To minimize this capacitance, narrow gate lines that are self-aligned with the FET channel are required. Here we describe a process for forming a printed self-aligned gate (Fig. 4A). After spin-coating the PMMA gate dielectric into the groove, the surface of the PMMA is rendered hydrophilic by a short, low-power oxygen plasma treatment. The substrate is then contacted with a flat, flexible stamp of poly(dimethyl siloxane) inked with a self-assembled monolayer of octyltrichlorosilane (OTS). The OTS is transferred onto the activated, hydrophilic PMMA only in the flat regions of the surface, rendering those surface regions hydrophobic, whereas the PMMA surface inside the embossed groove remains hydrophilic. This generates a surface-energy pattern used to direct inkjet-printed droplets of PEDOT to flow into the groove and to confine the gate electrode to the narrow groove (width $s = 10$ to 20 μm as defined in Fig. 4A), which is self-aligned with the embossed source and drain electrodes. When PEDOT droplets hit the surface in the vicinity of the groove, they deform from a spherical into an oval shape (Fig. 4B) by combined surface-energy and capillary forces, which attract them to flow into the

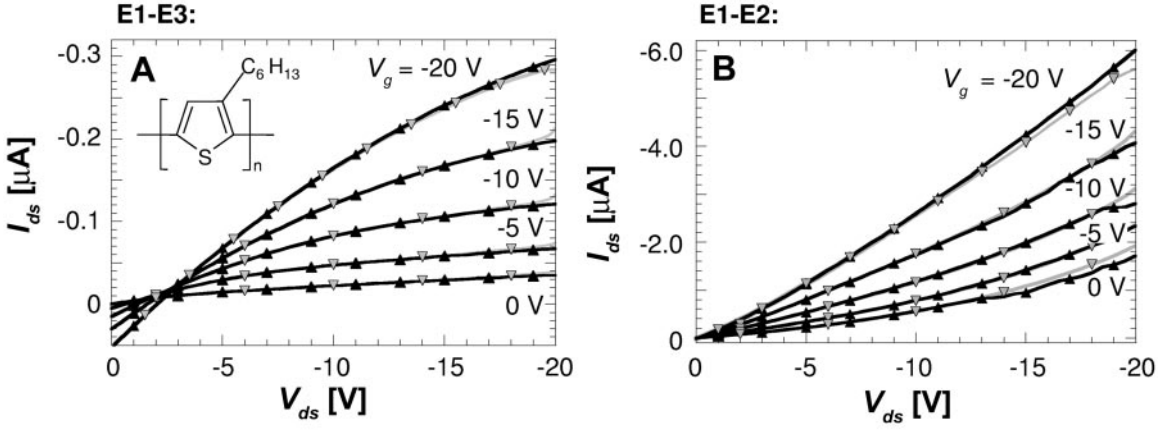

Fig. 3. Output characteristics of embossed P3HT devices. Successive measurements with increasing (upward-pointing triangles) and decreasing (downward-pointing triangles) source-drain voltages are shown. (**A**) Planar transistor with E1-E3 as source-drain electrodes (channel length, $L \approx 17$ μm; channel width, $W = 1$ mm). The inset in (A) shows the chemical structure of P3HT. (**B**) The corresponding vertical transistor with E1-E2 as source-drain electrodes ($L \approx 900$ nm; $W \approx 0.5$ mm).

groove. Atomic force microscopy showed no evidence for residual PEDOT in the flat regions of the surface (Fig. 4C). Control experiments with hydrophilic PMMA surfaces that had not been modified selectively with OTS have shown that on a wetting surface, capillary forces alone provide some, but less effective, confinement of droplets. In this way, we have fabricated operational planar and vertical embossed FETs with static device characteristics comparable to those of embossed FETS with unconfined gate electrodes. Capacitance-voltage measurements (Fig. 4D) show that the overlap capacitance per unit of channel width of embossed planar devices with a self-aligned PEDOT/PSS gate (s = 10 to 20 μm) is on the order of 0.3 to 0.5 pF/mm. This value is one order of magnitude lower than the overlap capacitance of 3 to 4 pF/mm of a planar polymer FET with an unconfined inkjet-printed PEDOT/PSS gate electrode of line width 60 to 80 μm (*6*).

Solid-state embossing combined with direct inkjet printing is a powerful manufacturing technique for fabricating solution-processed polymer FETs on flexible substrates. By direct-write printing of electrodes, we can deposit interconnects, active polymer islands, and via-hole interconnects (*6*). Embossing enables the controlled definition of submicrometer critical features. Our method for surface energy–assisted confinement of printed electrodes in embossed grooves to reduce overlap capacitance can be applied more generally, for example, to define ink-repelling barriers that enable the accurate printing of source-drain electrodes with small channel lengths (*6*) or to reduce the line width of interconnect lines. Self-aligned, submicrometer vertical-channel FETs with undegraded field-effect mobilities and reduced overlap capacitance will enable polymer integrated circuits with substantially improved switching speed (*2*).

Further downscaling of L in vertical-channel devices is possible. In our experiments, the minimum channel length was limited only by leakage currents through the dielectric PVP spacer layer. These became substantial at PVP thicknesses below 0.5 μm but were present even before embossing. To solve this problem, PET substrates with smaller surface roughness will be required. For very short channel devices, it will also become important to reduce frictional forces between the embossing master and the layers to be cut. Friction may force the top layers downward, along the indentation direction (*9*), but can be minimized by chemical modification of the master surface. Furthermore, selecting materials with $T_g \gg T_{emboss}$ will further prevent smearing and enhance the mechanical stability of the multilayer. Even in the planar device configuration, further downscaling can be realized, for example, by pressing the master into the multilayer only partially (by using shorter embossing cycles and/or reducing the applied load) or by decreasing the height of wedges of the embossing master. For instance, with a master of height h = 1.5 μm, microwires of gold and PEDOT separated by less than 1 μm have been demonstrated previously (*22*, *23*).

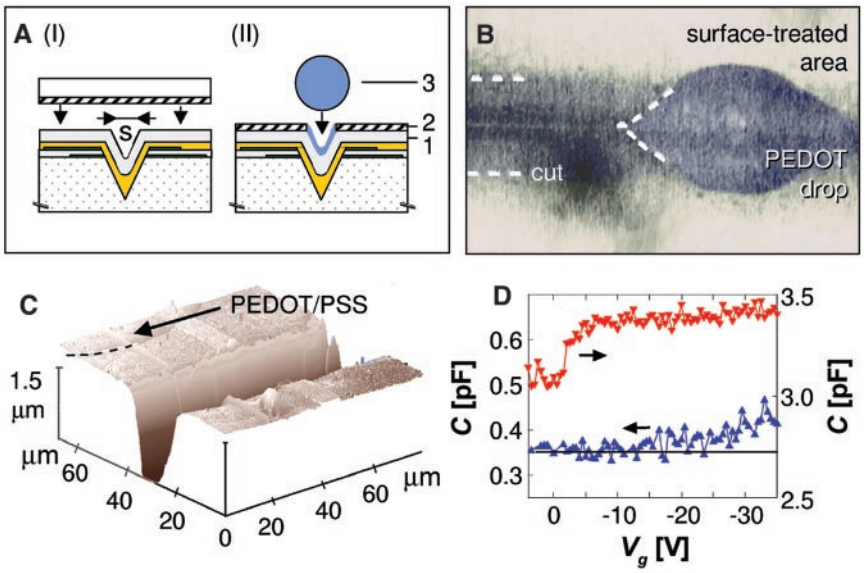

Fig. 4. Self-aligned printing of gate electrodes. (**A**) Selective inkjet deposition of a PEDOT/PSS gate electrode (3) with a self-assembled monolayer of OTS (2) deposited onto the flat surface regions of the hydrophilic PMMA gate dielectric (1). (**B**) Photograph of a liquid inkjet droplet of PEDOT/PSS impinging onto the substrate and being attracted into an embossed, surface-modified groove. Dashed lines indicate the edges of the groove and of the elongated droplet. (**C**) Atomic force micrograph of an embossed FET after surface energy–assisted gate printing into the groove. No traces of PEDOT/PSS were found directly next to the microgroove. The dashed line indicates the edge of a PEDOT droplet printed deliberately as a reference into the flat regions of the surface. (**D**) Capacitance-voltage characteristics of a self-aligned, embossed F8T2/PMMA FET (blue, measured against the left scale, with E1-E3 held at ground potential, W = 1000 μm, and s = 10 to 20 μm) and a conventional inkjet-printed planar FET (*6*) with an unconfined inkjet-printed PEDOT/PSS top-gate electrode (orange, measured against the right scale, with the source-drain grounded, W = 1000 μm, L = 5 μm, and a gate line width of 60 to 80 μm). As expected, a small increase of the capacitance in accumulation is seen in both cases. The very small capacitance of the self-aligned devices is close to the detection limit of our measurement setup (Fig. 2B).

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Materials and Methods

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