LETTERS

Coaxial silicon nanowires as solar cells and nanoelectronic power sources

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Solar cells are attractive candidates for clean and renewable power[1,2]; with miniaturization, they might also serve as integrated power sources for nanoelectronic systems. The use of nanostructures or nanostructured materials represents a general approach to reduce both cost and size and to improve efficiency in photovoltaics[1–9]. Nanoparticles, nanorods and nanowires have been used to improve charge collection efficiency in polymer-blend[4] and dye-sensitized solar cells[5,6], to demonstrate carrier multiplication[7], and to enable low-temperature processing of photovoltaic devices[3–6]. Moreover, recent theoretical studies have indicated that coaxial nanowire structures could improve carrier collection and overall efficiency with respect to single-crystal bulk semiconductors of the same materials[8,9]. However, solar cells based on hybrid nanoarchitectures suffer from relatively low efficiencies and poor stabilities[1]. In addition, previous studies have not yet addressed their use as photovoltaic power elements in nanoelectronics. Here we report the realization of p-type/intrinsic/n-type (p-i-n) coaxial silicon nanowire solar cells. Under one solar equivalent (1-sun) illumination, the p-i-n silicon nanowire elements yield a maximum power output of up to 200 pW per nanowire device and an apparent energy conversion efficiency of up to 3.4 per cent, with stable and improved efficiencies achievable at high-flux illuminations. Furthermore, we show that individual and interconnected silicon nanowire photovoltaic elements can serve as robust power sources to drive functional nanoelectronic sensors and logic gates. These coaxial silicon nanowire photovoltaic elements provide a new nanoscale test bed for studies of photo-induced energy/charge transport and artificial photosynthesis[10], and might find general usage as elements for powering ultralow-power electronics[11] and diverse nanosystems[12,13].

We have focused on p-i-n coaxial silicon nanowire structures (Fig. 1a) consisting of a p-type silicon nanowire core capped with i- and n-type silicon shells. An advantage of this core/shell architecture is that carrier separation takes place in the radial versus the longer axial direction, with a carrier collection distance smaller or comparable to the minority carrier diffusion length[8]. Hence, photogenerated carriers can reach the p-i-n junction with high efficiency without substantial bulk recombination. An additional consequence of this geometry is that material quality can be lower than in a traditional p-n junction device without causing large bulk recombination[1].

Silicon nanowire p-cores were synthesized by means of a nanocluster-catalysed vapour–liquid–solid (VLS) method[14,15]. Silicon shells were then deposited at a higher temperature and lower pressure than for p-core growth (Fig. 1a, right panel) to inhibit axial elongation of the silicon nanowire core during the shell deposition, where phosphine was used as the n-type dopant in the outer shell[15]. The growth temperatures were sufficiently low to ensure that minimal amounts of metal catalyst were incorporated into the silicon nanowire structure. Scanning electron microscopy (SEM) images of a typical p-i-n coaxial silicon nanowire recorded in the back-scattered electron mode (Fig. 1b) highlight several key features. First, the uniform contrast of the nanowire core is consistent with a single-crystalline structure expected for silicon nanowires obtained by the VLS method[14,15]. Second, contrast variation observed in the shells is indicative of a polycrystalline structure grain of the order of 30–80 nm. Third, the core/shell silicon nanowires have uniform

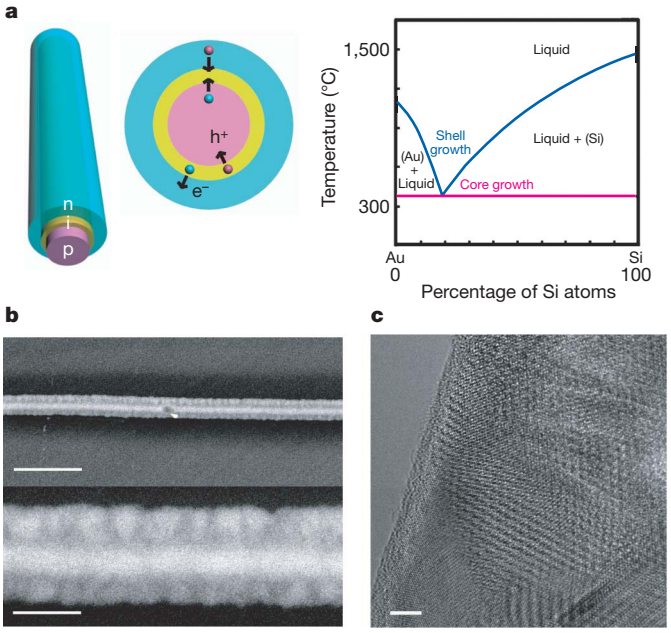

Figure 1 | Schematics and electron microscopy images of the p-i-n coaxial silicon nanowire. a, Illustrations of the core/shell silicon nanowire structure; its cross-sectional diagram shows that the photogenerated electrons (e^-) and holes (h^+) are swept into the n-shell and p-core, respectively, by the built-in electric field. The phase diagram of gold (Au)–silicon (Si) alloy on the right panel illustrates that the core is grown by means of the VLS mechanism, whereas the shells are deposited at higher temperature and lower pressure to inhibit further nanowire axial elongation. **b**, SEM images (back-scattered electron mode) of the p-i-n coaxial silicon nanowire at two different magnifications. Scale bar, 1 μm (top), 200 nm (bottom). The p-i-n silicon nanowire was grown with 100-nm-diameter gold catalyst, and with i- and n-shell growth times of 60 min and 30 min, respectively. The feeding ratios of silicon:boron and silicon:phosphorus are 500:1 and 200:1, respectively. **c**, High-resolution TEM image (spherical-aberration-corrected) of the p-i-n coaxial silicon nanowire. Scale bar, 5 nm.

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diameters of ~300 nm (280–360 nm for other nanowires), which is in agreement with independent transmission electron microscopy (TEM) and atomic force microscopy measurements. In addition, high-resolution TEM images (Fig. 1c) confirm that the nanowire shell is indeed polycrystalline. We note that this nanocrystalline shell structure could enhance light absorption in the nanowires (see below).

To characterize electrical transport through the p-i-n coaxial silicon nanowires, we fabricated metal contacts selectively to the inner p-core and outer n-shell (Fig. 2a). Briefly, core/shell silicon nanowires were etched selectively using potassium hydroxide (KOH) solution (see Methods) to expose the p-core in a lithographically defined region, and then metal contacts were made to the p-core and n-shell after a second lithographic patterning step, as shown in the SEM images of Fig. 2b. Dark current–voltage (I–V) curves obtained from devices fabricated in this way (Fig. 2c) exhibit several notable features. First, the linear I–V curves from core–core (p1-p2) and shell–shell (n1-n2) configurations indicate that ohmic contacts are made to both core and shell portions of the nanowires. Second, the I–V curve for the shell–shell contact reveals a shell

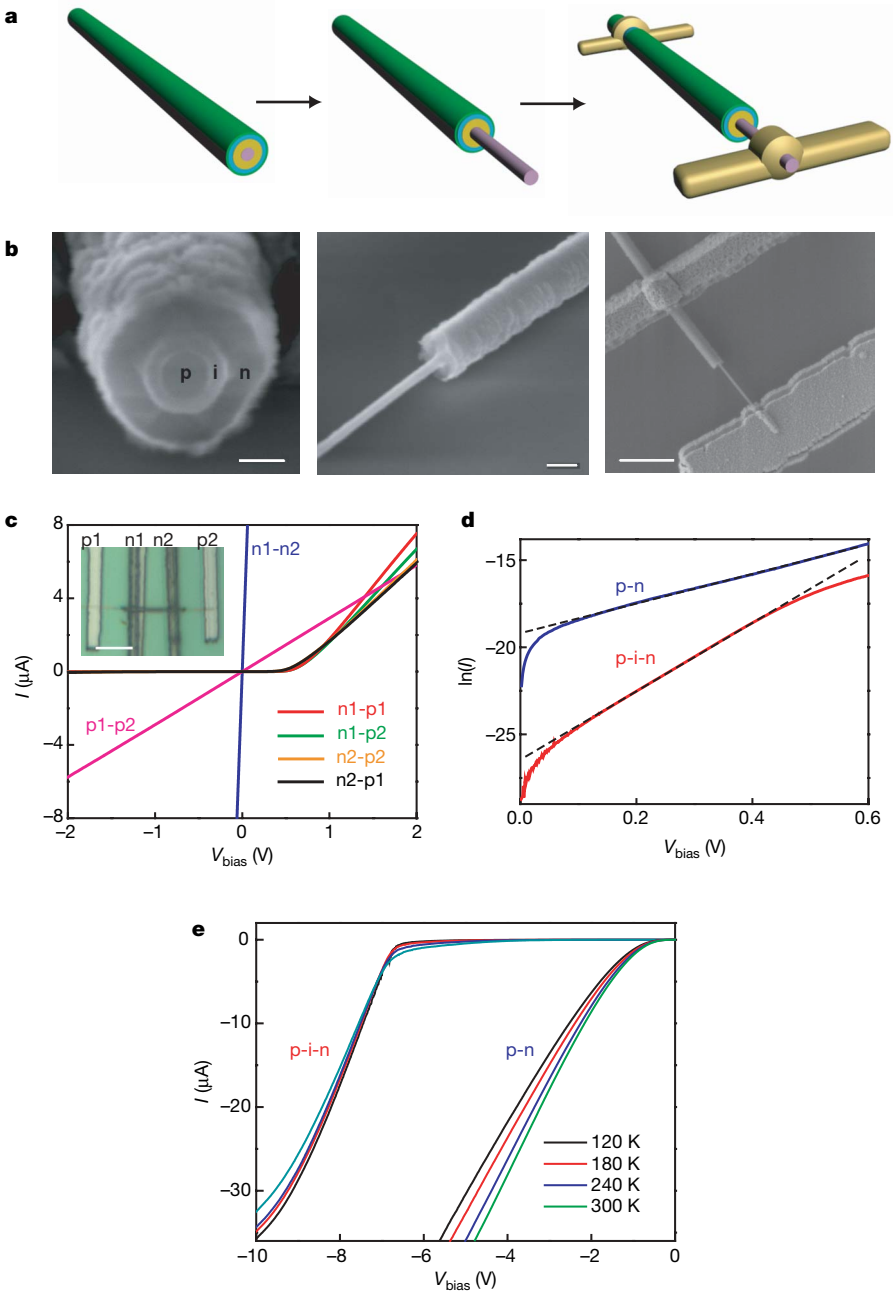

Figure 2 | Device fabrication and diode characterization. **a**, Schematics of device fabrication. Left, pink, yellow, cyan and green layers correspond to the p-core, i-shell, n-shell and PECVD-coated SiO_2, respectively. Middle, selective etching to expose the p-core. Right, metal contacts deposited on the p-core and n-shell. **b**, SEM images corresponding to schematics in **a**. Scale bars are 100 nm (left), 200 nm (middle) and 1.5 μm (right). **c**, Dark I–V curves of a p-i-n device with contacts on core–core, shell–shell and different core–shell combinations. V_{bias}, the applied bias voltage. Inset, optical microscope image of the device. Scale bar, 5 μm. **d**, Semi-log scale I–V curves of p-i-n and p-n diodes. The ideality factor N can be extrapolated (dashed lines) from the diode linear regimes (p-i-n diode, 0.12–0.50 V; p-n diode, 0.10–0.60 V), which are 1.96 and 4.52 for p-i-n and p-n diodes, respectively. To keep the total diameters of the p-n and p-i-n silicon nanowires approximately the same, the p-n silicon nanowire was grown with a 100-nm diameter gold catalyst and an n-shell growth time of 100 min. The SiH_4/dopants feeding ratios for p-n and p-i-n nanowires are the same (silicon:boron, 500:1; silicon:phosphorus, 200:1). **e**, Temperature-dependent I–V measurement of the p-n and p-i-n diodes in the reverse bias voltage regime.

conductance of 132 μS, higher than that of the core (3 μS); the calculated shell resistivity is within a factor of two of that measured for single-crystal n-type silicon nanowire prepared with a similar SiH_4:PH_3 ratio[15]. The highly conductive n-shell will reduce or eliminate potential drop along the shell, thereby enabling uniform radial carrier separation and collection when illuminated[8]. Third, *I*–*V* curves recorded from different core–shell contact geometries show rectifying behaviour, and demonstrate that the p-i-n coaxial silicon nanowires behave as well-defined diodes. The reproducibility of the selective etching and contact formation to p-cores and n-shells was further demonstrated by defining more complex 'AND' and 'OR' diode logic gates using single p-i-n coaxial silicon nanowires (Supplementary Fig. 1).

The core/shell silicon nanowire diodes were further characterized by analysing data recorded with and without the i-layer as a function of temperature. Fits to ln(*I*)–*V* data recorded in forward bias from p-i-n and p-n coaxial structures (Fig. 2d) are linear, and yield diode ideality factors *N* of 1.96 and 4.52, respectively (see Methods). The *N*-values show that introduction of the i-layer yields much better quality diodes. Reverse bias measurements from p-i-n and p-n diodes (Fig. 2e) also show markedly different behaviour: the p-i-n diode breaks down at much larger reverse-bias voltage (approximately −7 V) than the p-n diode (approximately −1 V) for all temperatures studied. In addition, the reverse-bias breakdown voltage of the p-n diode increases with decreasing temperature, which is consistent with a Zener (tunnelling) breakdown mechanism, whereas the breakdown voltage of the p-i-n structures exhibits little temperature dependence, suggesting contributions from tunnelling and avalanche mechanisms[16]. Overall, these results indicate that tunnelling or leakage currents are more significant in the p-n diode[17], and that the diode quality factor and breakdown behaviour are readily controlled during nanowire growth by the introduction of the i-layer as in planar structures[18,19].

The photovoltaic properties of the p-i-n coaxial silicon nanowire diodes were characterized under air mass 1.5 global (AM 1.5G) illumination. *I*–*V* data recorded from one of the better devices (Fig. 3a) yields an open-circuit voltage V_{oc} of 0.260 V, a short-circuit current I_{sc} of 0.503 nA and a fill factor F_{fill} of 55.0%. The maximum power output P_{max} for the silicon nanowire device at 1-sun (see Methods) is ~72 pW. Notably, these values were constant for measurements made over a seven-month period, thus demonstrating excellent stability of our nanowire photovoltaic elements. In addition, *I*–*V* data recorded using contacts to the n-shell that were 5.9 μm (n1) and 13.3 μm (n2) from the p-core contact (Fig. 3b) exhibited essentially the same photovoltaic response, thus indicating that the n-shell is equipotential with radial carrier separation occurring uniformly along the entire length of the core/shell silicon nanowire device. Measurements of I_{sc} as a function of the p-i-n coaxial silicon nanowire (Fig. 3c) length show linear scaling with values of 1 nA silicon nanowire^{-1} readily achieved for lengths of 10 μm (1-sun), whereas V_{oc} is essentially independent of length. The linear scaling of I_{sc} with silicon nanowire length suggests that photogenerated carriers are collected uniformly along the length of these radial nanostructures, and that scattering of light by the metal contacts does not make a major contribution to the observed photocurrent.

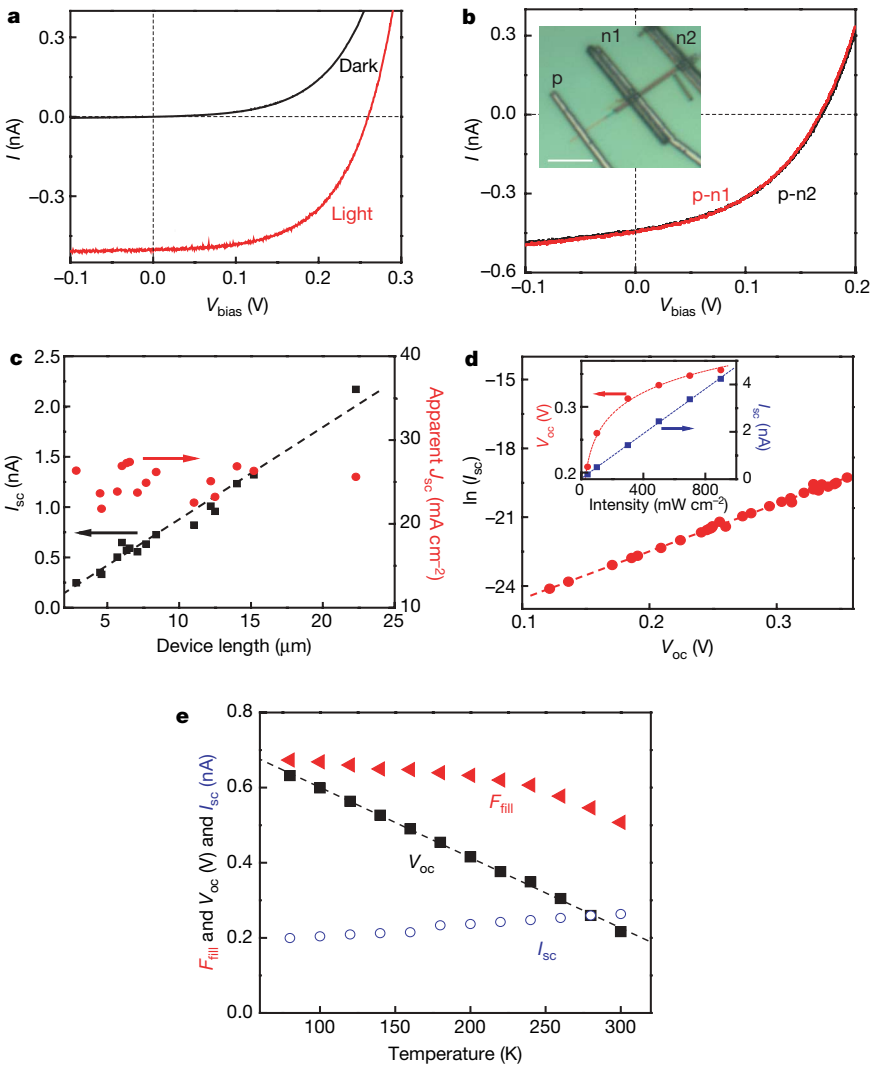

Figure 3 | Characterization of the p-i-n silicon nanowire photovoltaic device. **a**, Dark and light *I*–*V* curves. **b**, Light *I*–*V* curves for two different n-shell contact locations. Inset, optical microscopy image of the device. Scale bar, 5 μm. **c**, Device-length-dependent I_{sc} and J_{sc} (upper bound) plots. **d**, Plot of ln(I_{sc}) versus V_{oc}; each point corresponds to a different light intensity. Inset, light-intensity-dependent I_{sc} and V_{oc} plots. **e**, Temperature-dependent measurement. The device was illuminated at 0.6-sun to reduce sample heating, which may cause temperature fluctuations. The red triangle, black square and blue circle correspond to F_{fill}, V_{oc} and I_{sc}, respectively. The same device was characterized in **a**, **d** and **e**. The p-i-n coaxial silicon nanowire was grown using conditions as in Fig. 2.

The apparent short-circuit current density J_{sc} calculated using the projected area of the core/shell nanowire structure was $23.9 \pm 1.2\ mA\ cm^{-2}$ (upper bound, excluding metal covered and exposed p-core areas) and $16.0 \pm 0.8\ mA\ cm^{-2}$ (lower bound, including metal-covered and exposed p-core areas) for the device in Fig. 3a. The use of projected area to estimate the apparent current density is consistent with the methodology used with other nanostructured photovoltaic devices[3–6] and our use of devices as nanoscale power sources (see below, Fig. 4). Control experiments were also carried out to investigate the principal area of light absorption by devices. For example, measurements made on devices with and without lithographic masks that block illumination of the nanowire (Supplementary Fig. 2), with and without external scattering centres, and as a function of incident angle of illumination verify that the reported photocurrents and large apparent photocurrent densities arise primarily from direct nanowire absorption and are not much enhanced by scattering and/or waveguiding of incident light remote from devices. We note that the large nanowire J_{sc} values (Fig. 3c) imply substantial absorption across the solar spectrum. Such absorption is consistent with the nanocrystalline shell structure of the nanowires and previous studies of microcrystalline thin films[18], although the detailed nature of absorption will require further investigation. The apparent photovoltaic efficiency η of this device is $3.4 \pm 0.2\%$ (upper bound) and $2.3 \pm 0.2\%$ (lower bound), but might be improved through increased understanding of absorption and better coupling of light into the devices, for example, by vertical integration[8] or multilayer stacking[20].

I_{sc} and V_{oc} depend linearly and logarithmically, respectively, on the light intensity incident on the chip (inset, Fig. 3d), consistent with systematic increase in photogenerated carriers[19,21]. We note that the apparent efficiency is substantially higher at multiple-sun illumination: $4.1 \pm 0.2\%$ and $4.5 \pm 0.3\%$ (upper bounds) under 3-sun and 5-sun conditions, respectively. Although this apparent efficiency enhancement is larger than that in a planar silicon solar cell[19], it is consistent with the larger ideality factor (N) and lower 1-sun V_{oc} of the nanowire devices[19]. Analysis of a plot of $\ln(I_{sc})$ versus V_{oc} (Fig. 3d) yields values of the diode ideality factor and saturation current of $N = 1.86$ and $I_0 = 2.72$ pA, respectively (see Methods). These values are similar to those extrapolated from the dark measurements ($N = 1.96$, $I_0 = 3.24$ pA), and thus demonstrate good consistency in the behaviour and analysis of these core/shell silicon nanowire diode devices.

In addition, the temperature dependences of I_{sc}, V_{oc} and F_{fill} were characterized to understand better the behaviour of the silicon nanowire photovoltaic devices (Fig. 3e). I_{sc} decreases slightly with decreasing temperature, and can be attributed to reduced light absorption due to increasing bandgap as temperature is reduced[22]. V_{oc} exhibits a substantial linear increase with decreasing temperature, where the slope (dV_{oc}/dT) of $-1.9\ mV\ K^{-1}$ is close to the value ($-1.7\ mV\ K^{-1}$) calculated in single crystalline silicon solar cells[21]. The observed increase in V_{oc} can be attributed to a reduced recombination rate at lower temperature[21,22], and yields an apparent efficiency of 6.6% (upper bound) at 80 K (0.6-sun). The F_{fill} also increases with decreasing temperature (as expected from the negative dV_{oc}/dT)[22]. Taken together, these V_{oc} and F_{fill} results indicate that the silicon nanowire photovoltaic performance at room temperature (298 K in our experiments) can be significantly improved by reducing recombination processes, for example, by improving the crystalline structure of the shells and/or passivating the nanowire surface and grain boundaries[19,23].

Our core/shell silicon nanowire results can be compared to nanocrystal-based[4] and nanorod-based[5,6] photovoltaic devices. The best silicon nanowire device exhibits large apparent short-circuit current densities—$23.9\ mA\ cm^{-2}$ (upper bound) and $16.0\ mA\ cm^{-2}$ (lower bound)—with upper limits that are comparable to the $24.4\ mA\ cm^{2}$ value for the best thin film nanocrystalline silicon solar cell[24], and substantially better than values reported for CdSe nanorod/poly-3-hexathiophene[4] and dye-sensitized ZnO nanorod[5,6] solar cells. The V_{oc} value, 0.260 V, is 2–2.8 times lower than reported in these previous studies[4–6,24] and represents an area that should be addressed in future studies. However, the overall apparent efficiency of the p-i-n coaxial silicon nanowire photovoltaic elements—3.4% (upper bound) and 2.3% (lower bound)—exceeds reported nanorod/polymer and nanorod/dye systems[4–6], and could be increased substantially with improvements in V_{oc} by means of, for example, surface passivation. In addition, increasing the illumination intensity can yield stable improvements in the apparent efficiency of our p-i-n coaxial silicon nanowire photovoltaic elements in contrast to other nanostructured solar cells, which often exhibit degradation[4–6].

The ability of individual core/shell silicon nanowires to function as robust photovoltaic elements might indicate their potential as nanoscale power sources that might be integrated 'on-chip' with other

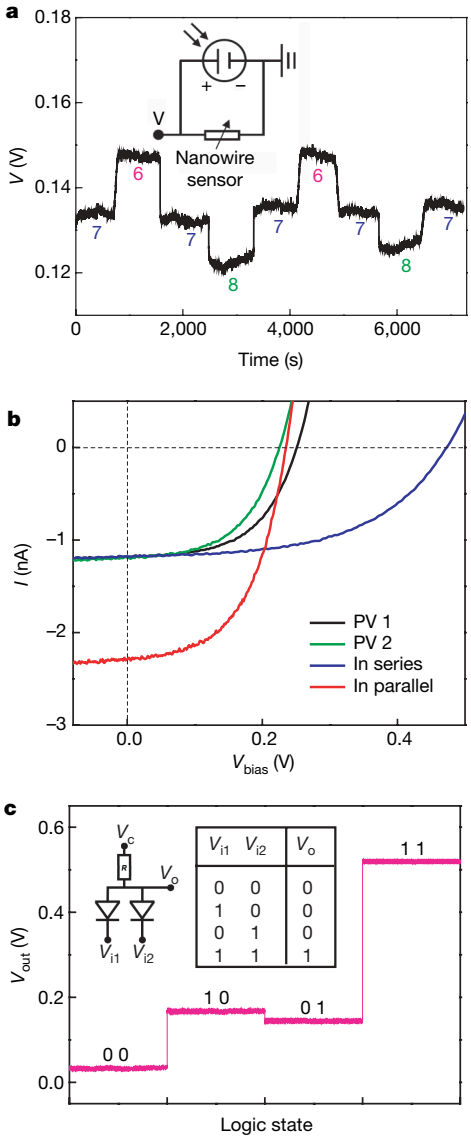

Figure 4 | Self-powered nanosystems. a, Real-time detection of the voltage drop across an aminopropyltriethoxysilane-modified silicon nanowire at different pH values. The silicon nanowire pH sensor is powered by a single silicon nanowire photovoltaic device operating under 8-sun illumination ($V_{oc} = 0.34$ V, $I_{sc} = 8.75$ nA). Inset, circuit schematics. **b**, Light I–V curves (1-sun, AM 1.5G) of two silicon nanowire photovoltaic devices (PV 1 and PV 2) individually and connected in series and in parallel. **c**, Nanowire AND logic gate powered by two silicon nanowire photovoltaic devices in series. Insets, circuit schematics and truth table for the AND gate. The resistance of CdSe nanowire is ~5 GΩ; the V_{oc} of two photovoltaic devices in series is 0.53 V. The large resistance of the CdSe nanowire and reverse-biased p-i-n diode makes V_c and V_i (HIGH) very close to V_{oc} of the photovoltaic device. To get V_i (LOW), the diode is simply grounded.

semiconductor nanowire- and carbon-nanotube-based nanoelectronic elements, given that these elements require power as low as a few nanowatts[25–27]. Recent work addressing this key issue has involved the use of piezoelectric ZnO nanowires for mechanical-to-electrical conversion, although the direct current (d.c.) power developed by this nanogenerator[28,29], 1–4 fW per nanowire, is at present less than is needed to drive nanoelectronic devices. Silicon nanowire photovoltaic elements can produce 50–200 pW per nanowire at 1-sun illumination, and thus could function as nanoscale power supplies for nanoelectronics by either increasing the light intensity or using several coupled elements. For example, a single silicon nanowire photovoltaic device, operating under 8-sun illumination (P_{max} = 1.86 nW, η = 4.8%) was used to drive a silicon nanowire pH sensor[25] without additional power (Fig. 4a). Measurements of the voltage drop across the p-type silicon nanowire sensor (powered solely by the silicon nanowire photovoltaic element) as a function of time (Fig. 4a) show reversible increase (or decrease) in voltage as the solution pH is decreased (or increased) that are consistent with the expected changes in resistance of the silicon nanowire with surface charge[25]. In addition, we note that the photovoltaic (under constant 8-sun illumination) and sensor devices both exhibited excellent stability over the approximately two-hour time of experiments.

Last, the core/shell silicon nanowire photovoltaic devices were interconnected in series and in parallel to demonstrate scaling of the output characteristics and to drive larger loads. *I–V* data recorded from two illuminated silicon nanowire elements (Fig. 4b) show several important features. First, the individual elements exhibit very similar behaviour, highlighting the good reproducibility of our core/shell nanowire devices. Second, interconnection of the two elements in series and parallel yields V_{oc} and I_{sc} values, respectively, that are approximately the sum of two, as expected. Notably, we have used interconnected silicon nanowire photovoltaic elements as the sole power supply driving a nanowire-based AND logic gate (Fig. 4c), where V_c and the voltage inputs 1 and 2 V_{i1} (HIGH) and V_{i2} (HIGH) are provided by two nanowire photovoltaic devices in series at 2-sun illumination. (HIGH is the input state and V_{i1} (HIGH) and V_{i2} (HIGH) are close to V_{oc} of the PV devices.) A summary of the input/output results (right inset, Fig. 4c) shows correct AND logic. This work thus demonstrates the potential for self-powered nanowire-based logic circuits and, more generally, the possibility of self-powered functional nanoelectronic systems through, for example, the integration of multiple stacked silicon nanowire photovoltaic elements with nanoelectronic, photonic and biological sensing devices.

METHODS SUMMARY

Single-crystalline silicon nanowire p-cores were synthesized by means of a nanocluster-catalysed VLS method[14,15], and then chemical vapour deposition was used to deposit i- and n-type nanocrystalline silicon shells; shell growth was carried out at higher temperature and lower pressure than those used in core growth to inhibit axial elongation of the silicon nanowire core. After nanowire growth, SiO_2 was deposited conformally by means of plasma-enhanced chemical vapour deposition (PECVD). Standard electron beam lithography, silicon wet chemical etching (KOH etchant) and thermal evaporation were used to make coaxial nanowire devices, with selective contacts on the p-core and n-shell. A standard solar simulator (150 W, Newport Stratford) with an AM 1.5G filter was used to characterize the photovoltaic device response, where the average intensity was calibrated using a power meter. For multiple-sun illumination, an aspheric lens was placed between the light source and nanowire devices. All electrical measurements were made with a probe station (TTP-4, Desert Cryogenics). For self-powered pH sensing and AND logic gate experiments, a computer-controlled analogue-to-digital converter (6030E, National Instruments) was used to record the voltage drop or voltage output of the silicon nanowire devices.

Full Methods and any associated references are available in the online version of the paper at www.nature.com/nature.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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METHODS

Nanowire synthesis. p-i-n coaxial silicon nanowires were prepared using 100-nm gold nanoclusters as catalysts, silane (SiH_4) as the silicon reactant, diboron (B_2H_6, 100 p.p.m. in H_2) as the p-type dopant, phosphine (PH_3, 1,000 p.p.m. in H_2) as the n-type dopant, and hydrogen (H_2) as the carrier gas. For the p-core nanowire growth, the flow rates of SiH_4, B_2H_6 and H_2 were 1, 10 and 60 standard (converted to standard temperature and pressure) cubic centimetres per minute, respectively. For the i-shell deposition, the flow rates of SiH_4 and H_2 were 0.15 and 60 standard cubic centimetres per minute, respectively, and 0.75 standard cubic centimetres per minute of PH_3 was added during the subsequent n-shell deposition. The growth temperatures for core and shells were 440 °C and 650 °C, respectively; the total pressures were 40 torr and 25 torr, respectively. The p-core growth lasted 3 h, and the deposition of i- and n- shells took 1 h and 0.5 h, respectively. Following the growth, the nanowire growth substrate was cleaned by oxygen plasma and the SiO_2 hard mask (30–60-nm thick) was deposited conformally onto the silicon nanowire surface by means of PECVD.

Device fabrication. All p-i-n devices were fabricated on heavily doped silicon substrates with 100 nm thermal oxide and 200 nm silicon nitride (n-type, resistivity $<0.005\,\Omega$ cm, Nova Electronic Materials). To fix the nanowires, chromium pads were patterned by electron beam lithography (EBL) and deposited directly on the SiO_2 hard mask by thermal evaporation. The second EBL step defined an etching window to expose the p-core in selected regions. The SiO_2 at the exposed nanowire region was first etched away using buffered HF with the e-beam resist as an etching mask, and the underlying shells of the silicon nanowire were further removed by KOH etching (70 °C, 45 s). In the last step, titanium/palladium contacts (3 nm/500 nm thick) at the p-core and n-shell of individual silicon nanowires were patterned by EBL and deposited by thermal evaporation. No annealing was required to ensure ohmic contact formation.

Sample illumination. A standard solar simulator (150 W, Newport Stratford) with an AM 1.5G filter was used in our experiments, in which the average intensity was calibrated using a power meter. For multiple-sun illumination, an aspheric lens was placed between the light source and the nanowire photovoltaic device. It should be noted that the exact light intensity incident on the nanowire cannot be measured exactly because its physical dimensions (around 300 nm in diameter and 3–22 μm in length) are orders of magnitude smaller than those of the pin hole of a power meter (millimetre range). Nevertheless, the intensity should be fairly close to 1-sun according to the light intensity uniformity guaranteed by the solar simulator vendor.

***I–V* data analysis.** The saturation current, I_0, together with the diode ideality factor N was extrapolated from the dark I–V curve using the ideal diode equation:

$$\ln(I) = \frac{q}{NkT} V + \ln(I_0)$$

where q is the electronic charge and k is the Boltzmann constant. The average $\pm 1\sigma$ ideality factor values obtained from the analysis of p-i-n and p-n coaxial silicon nanowire were 2.23 ± 0.13 and 4.70 ± 0.77, respectively. Under illumination, the ideal diode equation can be expressed in terms of I_{sc} and V_{oc} as:

$$\ln(I_{sc}) = \frac{q}{NkT} V_{oc} + \ln(I_0)$$

where fits to $\ln(I_{sc})$ versus V_{oc} (for example, Fig. 3d) are used to determine N and I_0 from the slope and intercept, respectively.

Silicon nanowire photovoltaic-powered nanowire sensor and logic devices. p-type silicon nanowire (diameter, 20 nm; Si:B = 16,000:1) sensor devices (Fig. 4a) were fabricated as described elsewhere[30]. The sensor devices were modified with aminopropyltriethoxysilane in ethanol/H_2O (95%/5%), and a single polydimethylsiloxane microfluidic channel was used to deliver different pH solutions during the experiments[30]. The silicon nanowire sensor resistance (10–30 MΩ) was chosen to allow for operation in the high-power working regime of the photovoltaic device in which the output voltage ranges from one-third to one-half of V_{oc} but the output current is relatively constant. The p-contact of the silicon nanowire photovoltaic device was connected to one end of the sensor device, whereas the n-contact and the other end of the sensor device were grounded, and a computer-controlled analogue-to-digital converter (6030E, National Instruments) was used to record the voltage drop across the silicon nanowire sensor. The self-powered AND gate (Fig. 4c) was made entirely from nanowires, in which p-i-n coaxial silicon nanowires were configured as the two diodes and a CdSe nanowire was used as the resistor. The large resistance of the CdSe nanowire and reverse-biased p-i-n diodes yielded V_c and V_i (HIGH) values close to the V_{oc} (0.53 V) of the photovoltaic device (two p-i-n coaxial silicon nanowire elements in series). Voltage outputs for all logic gate devices were recorded using a computer-controlled analogue-to-digital converter.

30. Patolsky, F., Zheng, G. F. & Lieber, C. M. Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species. *Nature Protocols* **1**, 1711–1724; doi:10.1038/nprot.2006.227 (2006).